AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions, listing, of claims in the specification.

LISTING OF CLAIMS:

Claim 1 (original) An on-system programmable and off-system programmable chip comprising:

a control circuit;

an off-system programmable nonvolatile memory connected to said control circuit for being programmable only when connected to an external programming voltage;

an on-system programmable nonvolatile memory connected to said control circuit for being programmable under control of said control circuit;

a pumping circuit connected to said on-system programmable nonvolatile memory for supplying an internal programming voltage during programming said on-system programmable nonvolatile memory;

a volatile memory connected to said control circuit; and

an I/O unit connected to said control circuit.

Claim 2 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises a one-time programmable memory array.

Claim 3 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises a multi-time programmable memory array.

Claim 4 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises an electrically erasable programmable memory array.

Claim 5 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises a flash memory array.

Claim 6 (original) The chip of claim 1, wherein said on-system programmable nonvolatile memory comprises an electrically erasable programmable memory array.

Claim 7 (original) The chip of claim 1, wherein said on-system programmable nonvolatile memory comprises a flash memory array.

Claim 8 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory and on-system programmable nonvolatile memory are spatially separated.

Claim 9 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory and on-system programmable nonvolatile memory are selected from a memory block.

Claim 10 (original) The chip of claim 9, further comprising a switch for connecting said on-system programmable nonvolatile memory to said internal programming voltage.

Claim 11 (original) The chip of claim 10, wherein said switch comprises a fuse.

Claim 12 (original) The chip of claim 10, wherein said switch comprises a programmed circuit.

Claim 13 (original) The chip of claim 10, wherein said switch is connected to said control circuit for determining said off-system programmable nonvolatile memory or on-system programmable nonvolatile memory to be assigned.

Claim 14 (original) The chip of claim 1, wherein said volatile memory comprises a static random access memory.

Claim 15 (original) The chip of claim 7, further comprising a state machine connected to said on-system programmable nonvolatile memory for preventing said on-system programmable nonvolatile memory from over erasing.

Claim 16 (original) The chip of claim 7, wherein said flash memory array comprises a plurality of memory cells each including a flash cell connected with a MOS transistor for preventing said flash cell from over erasing.

Claim 17 (original) The chip of claim7, wherein said control circuit executes a state machine program for preventing said on-system programmable nonvolatile memory from over erasing.

Claim 18 (original) The chip of claim 17, wherein said state machine program is programmed in said off-system programmable nonvolatile memory.

Claim 19 (original) The chip of claim 17, wherein said state machine program is stored in said volatile memory.

Claim 20 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory has a first capacity and said on-system programmable nonvolatile memory has a second capacity less than said first capacity.

Claim 21 (original) The chip of claim 1, wherein said on-system programmable nonvolatile memory includes a plurality of programming units.

Claim 22 (original) The chip of claim 21, wherein each of said plurality of programming units comprises a memory cell.

Claim 23 (original) The chip of claim 21, wherein each of said plurality of programming units comprises is a bit.

Claim 24 (original) The chip of claim 21, wherein each of said plurality of programming units comprises a byte.

Claim 25 (original) The chip of claim 21, wherein each of said plurality of programming units comprises a word.

Claim 26 (original) The chip of claim 6, wherein said control circuit programs a desired amendment content that is read in from said I/O unit and sent to said on-system programmable nonvolatile memory.

Claim 27 (original) The chip of claim 7, wherein said control circuit reads a content out from said on-system programmable nonvolatile memory, stores said content to said volatile memory, amends a portion of said content to obtain an amended content, and programs said amended content to said on-system programmable nonvolatile memory.

Claim 28 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory includes a program code for operation of said control circuit.

Claim 29 (original) The chip of claim 1, wherein said off-system programmable nonvolatile memory includes a control process for said control circuit to program said on-system programmable nonvolatile memory.

Claim 30 (original) The chip of claim 1, wherein said on-system programmable nonvolatile memory is programmable under an operation mode.

Claim 31 (original) The chip of claim 1, wherein said on-system programmable nonvolatile memory includes a data code.

Claims 32-39 (canceled).

Claim 40 (original) A method for forming an on-system programmable and off-system programmable chip, comprising the steps of :

forming a control circuit in said chip;

connecting an off-system programmable nonvolatile memory to said control circuit;

connecting an on-system programmable nonvolatile memory to said control circuit;

connecting a pumping circuit to said on-system programmable nonvolatile memory;

connecting a volatile memory to said control circuit; and

connecting an I/O unit to said control circuit;

wherein said off-system programmable nonvolatile memory is programmable by connecting with an external programming voltage from outside of said chip, and said on-system programmable nonvolatile memory is programmable by supplying an internal programming voltage from said pumping circuit.

Claim 41 (original) The method of claim 40, further comprising programming a program code for operating said control circuit to said off-system programmable nonvolatile memory.

Claim 42 (original) The method of claim 40, further comprising connecting a state machine to said on-system programmable nonvolatile memory for preventing said on-system programmable nonvolatile memory from over erasing.

Claim 43 (original) The method of claim 40, further comprising programming a data code to said off-system programmable nonvolatile memory.

Claim 44 (original) The method of claim 40, further comprising programming a state machine program to said off-system programmable nonvolatile memory for preventing said on-system programmable nonvolatile memory from over erasing.

Claim 45 (original) The method of claim 40, further comprising dividing a memory block into said on-system programmable nonvolatile memory and off-system programmable nonvolatile memory.

Claim 46 (original) The method of claim 40, wherein the step of connecting a pumping circuit to said on-system programmable nonvolatile memory comprises closing a switch between said pumping circuit and on-system programmable nonvolatile memory.

Claim 47 (original) The method of claim 40, further comprising programming a control process for said control circuit to operate said on-system programmable nonvolatile memory to said off-system programmable nonvolatile memory.

Claim 48 (original) The method of claim 40, further comprising programming a data code to said on-system programmable nonvolatile memory.

Claim 49 (original) The method of claim 40, further comprising programming a program code other than for operating said control circuit to said on-system programmable nonvolatile memory.